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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,880	03/22/2004	Uday Shah	P18611	9870

25694 7590 09/21/2004

INTEL CORPORATION
P.O. BOX 5326
SANTA CLARA, CA 95056-5326

EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,880	SHAH ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-16 and 18* is/are rejected.

7)☒ Claim(s) *9,17 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification objection

1. The disclosure is objected to because of the following informalities: page 7 line 6 "100" to read --110-- to maintain consistency with drawings and specs.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to date of application for patent in United States.

3. Claims 1 – 4 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. (US Patent 6306715).

4. Chan et al. teach a method for making a semiconductor device comprising:

forming a dielectric layer (14) on a substrate (10), forming a metal layer (16, 18) on the dielectric layer, forming on the metal layer a masking layer (24) that has first and second sides, and then lining the first and second sides of the masking layer with a sacrificial layer (28);

wherein the dielectric layer comprises a high-k gate dielectric layer selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, yttrium oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium

strontium titanium oxide, barium titanium oxide, strontium titanium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate (col. 2 lines 55 – 58);

wherein the metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide (col. 2 line 59 – col. 3 line 20);

etching the metal layer and the dielectric layer after lining the first and second sides of the masking layer with the sacrificial layer (fig. 3), and removing the sacrificial layer after the metal layer is etched (col. 3 line 28 – col. 4 line 19); and

wherein the sacrificial layer comprises a material that is selected from the group consisting of silicon nitride, a carbon doped silicon nitride, and silicon dioxide, and the first and second sides of the masking layer are lined with the sacrificial layer by depositing the sacrificial layer onto the metal layer, and onto the first and second sides of the masking layer, then applying an anisotropic plasma dry etch process to remove the sacrificial layer from the metal layer (col. 3 lines 28 – 60).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 6, 7, and 10 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US Patent 6306715) in view of Samavevedam et al. (USPAP 2004/0023478).

7. Chan et al. teach features previously outlined, but lack forming a first metal layer on a first part of the dielectric layer, leaving a second part of the dielectric layer exposed, forming a second metal layer on the first metal layer and on the second part of the dielectric layer, forming on the second metal layer a masking layer that has first and second sides;

wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV;

wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 ~eV; and

wherein the masking layer comprises polysilicon.

8. However, Samavedam et al. teach the steps of forming a first metal layer (110) on a first part of the dielectric layer, leaving a second part of the dielectric layer exposed (fig. 2), forming a second metal layer (114) on the first metal layer and on the second part of the dielectric layer, forming on the second metal layer a masking layer (116, 118) that has first and second sides;

wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV (paragraph 22, 27);

wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 ~eV (paragraphs 25, 27); and

wherein the masking layer comprises polysilicon (paragraph 26).

9. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Samavedam et al. into the Chan et al. reference to form a high-K gate dielectric with reduced damage.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US Patent 6306715) in view of Matsuo (USPAP 2004/0000695).

11. Chan et al. teach the features previously outlined, but lacks the steps of forming a first metal layer on the high-k gate dielectric layer, removing part of the first metal layer, forming a second metal layer on the first metal layer and on the high-k gate dielectric layer, a first part of the second metal layer covering the remaining part of the first metal layer and a second part of the second metal layer covering the high-k gate dielectric layer, forming a polysilicon layer on the second metal layer, and removing part of the polysilicon layer to generate a patterned polysilicon layer that has first and second sides and to expose a third part of the second metal layer.

12. However, Matsuo teaches a method for making a semiconductor device comprising;

forming a high-k gate dielectric layer on a substrate, forming a first metal layer on the high-k gate dielectric layer (fig. 6A);

removing part of the first metal layer (203) to expose part of a high K gate dielectric (fig. 6B);

forming a second metal layer (205) on the first metal layer and on the high-k gate dielectric layer (202), a first part of the second metal layer covering the remaining part of the first metal layer and a second part of the second metal layer covering the high-k gate dielectric layer (fig. 6C), forming a polysilicon layer (206) on the second metal layer; and

removing part of the polysilicon layer to generate a patterned polysilicon layer that has first and second sides, and to expose a third part of the second metal layer (fig. 7A).

13. Therefore, it would have been obvious to one of ordinary skill in the art time invention was made to incorporate the teachings of Matsuo into the Chan et al. reference to fabricate a self-aligned dual metal gate transistor.

14. Claims 9, 17, and 19 are objected to as being dependent upon a rejected claim, but would be allowable if rewritten in independent form.

15. Prior art considered, but not used in the rejection include Weybright et al. (US Patent 6403423), Nallan et al. (USP AP 2003/0180968), Lee (US Patent 2003/0198104), Hobbs et al. (US Patent 6432779), and Signorini (US Patent 6484989).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from the Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2825

IA

September 15, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800